VLSI Design of Low Power Reversible 8-bit Barrel Shifter

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***Abstract*—Nowadays reversible circuit designing is the emerging area of research. This design strategy aims towards the formation of digital circuits with ideally zero power dissipation. And also Reversible logic is gaining interest in the recent past Due to its less heat dissipating characteristics. A lot of research has been done in combinational as well as sequential design of reversible circuits. In this paper we have proposed a reversible fredkin gate which is better than the existing designs in the literature. A novel design of reversible 8-bit barrel shifter proposed in this paper. The important reversible gates used for reversible logic synthesis are Feynman gate, Fredkin gate, TSG gate and sayem gate etc.The transistorized implementation of reversible gate presented in this paper are completely reversible in nature i.e. it can perform both forward and backward computation.Layouts for each gate and power, delay,PDP and LVS done through Tanner EDA tools .**

Keywords—Reversible Logic; Reversible Gate; Power Dissipation; Flip-Flop, Garbage.

I. INTRODUCTION

Conventionally digital circuits were designed using basic logic gates. These conventional basic logic gates dissipate some energy loss due to the information loss during the operation [1]. Irreversibility of energy is caused because the total number of output signals in the conventional gate is less than the number of total input signals. Reduced number of output signals is the major cause of the lowering of entropy of the overall digital system. The amount of energy loss for one bit of information loss in an irreversible gate was given by R. Landauer in 1961. Later in 1973 C. H. Bennette has shown that this energy loss can be minimized or even removed if the circuit is made up from the reversible logic gates [2].Reversible circuit designing is gaining wide scope in the area of Quantum computing, Low power CMOS design, Nanotechnology, Optical computing, Signal processing, Advanced computing etc due to its ability to design low loss or approximately loss less digital circuits. Reversible logic concept is based on the formulation of the input states of the digital logic system by knowing its output states at any moment, whereas we can generate the output states from input in a conventional digital system.

Reversible logic approach converts any irreversible digital circuit in reversible circuit by replacing conventional logic gates with new reversible gates. This approach optimizes the circuit on the basis of total number of reversible gates used in the designing. The key issues of reversible circuit designing, apart from fewer gates are the minimization of garbage output signals generated, quantum cost etc [3-6].

II. FUNDAMENTALS OF REVERSIBLE LOGIC

Reversible logic is a concept of digital circuit design which was born with the concept of creating digital logic circuits with zero power dissipation. It replaces irreversible logic gates with reversible gates in the conventional digital circuits. Some basic concepts of reversible logic are as follows:

Reversible gates are denoted as (n, n) digital logic gates, where (n, n) can be elaborated as (Total number of input signals, Total number of output signals). In reversible logic gates both the number of input signals and the number of output signals are equal. In these gates we can generate the input combinations at any instance by knowing the output combinations only. There exists a one to one mapping between the input and output signals i.e. a unique output combination occurs for individual input combinations.

Generally reversible gates follow these norms-

- Total number of input signals = Total number of output signals.
- One to one mapping between input and output variables.
- No feedback.
- Individual output bits are high for a total of half the number of total input combinations.

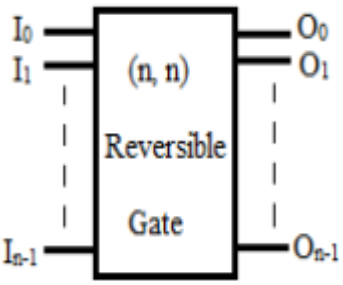


Figure 1. Block diagram of (n, n) Reversible logic gate

III. REVERSIBLE LOGIC GATES

A. *FEYNMAN GATE*

Fig. 1 shows a Feynman Gate. Feynman Gate (FG) can be used as a copying gate. Since a fan-out is not allowed in reversible logic, this gate is useful for duplication of the required outputs.

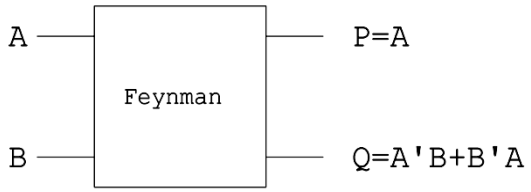


Figure 2. Feynman gate

1) *TRANSISTOR IMPLEMENTATION:*

Fig. 3 shows the transistor implementation of the Feynman gate.The transistor implementation is fully reversible, that is, the given circuit can also work for forward as well as reverse operation.

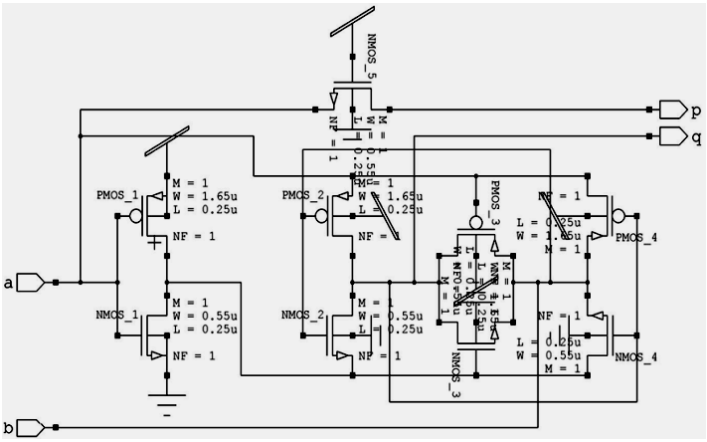


Figure 3. Reversible Transistor Implementation of the Feynman gate.

2) *LAYOUT:*

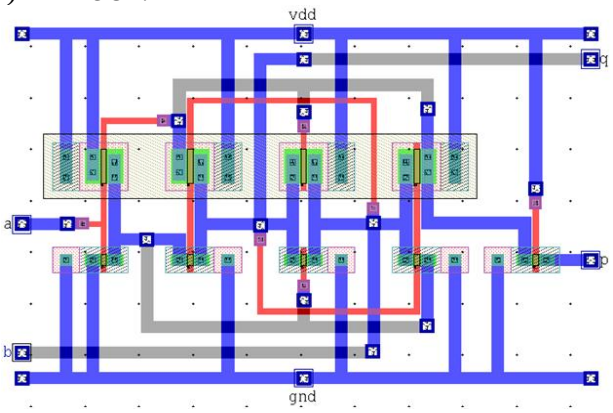


Figure 4. Layout of Reversible Feynman gate.

B. *FREDKIN GATE*

Fig. 5 shows a 3*3 Fredkin gate. The input vector is I(A,B,C) and the output vector is 0(P,Q,R).The output is defined by P=A, Q=A'B+AC and R=A'C +AB.

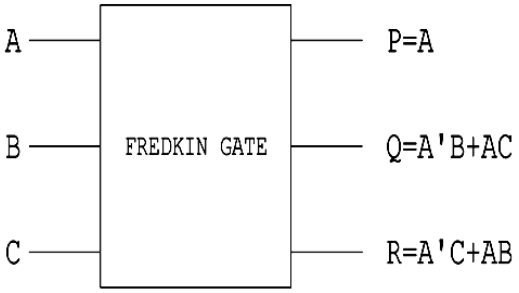


Figure 5. Fredkin gate

1) *TRANSISTOR IMPLEMENTATION:*

Fig. 6 shows the transistor implementation of the Fredkin Gate that need only four transistors. In the implementation the output P is directly taken from input A as output P is same as input A. The proposed transistor implementation is suitable both for forward as well as ackward computation ,i.e. completely reversible in nature. The forward and backward computations for Fredkin gate are explained below.

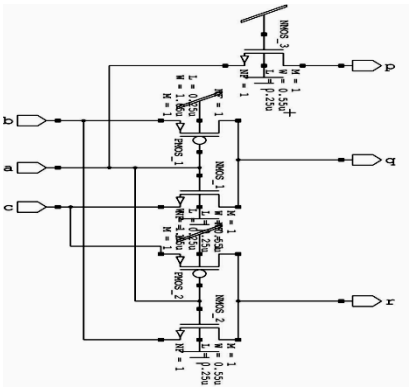


Figure 6. Reversible Transistor Implementation of the Fredkin gate

2) *LAYOUT:*

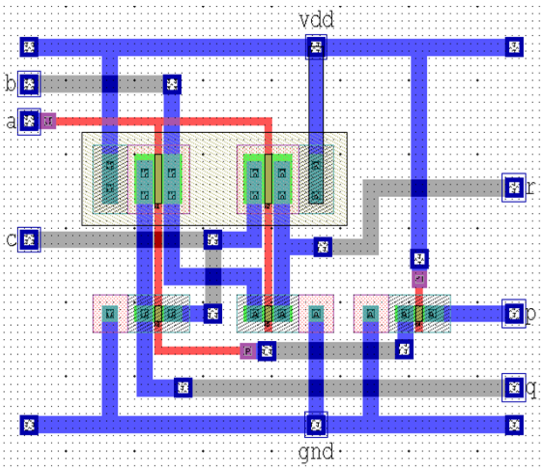


Figure 7. Layout of Reversible Fredkin gate.

3) *2:1 Reversible Multiplexer:*

A 3x3 reversible fredkin gate is proposed in order to function as the 2:1 reversible multiplexer producing two garbage bits. The inputs are S, A and B. Based on the selection input S, the corresponding message bits are passed on to the output Y. Figure depicts the symbolic representation of fredkin gate and Table I describes its truth table.

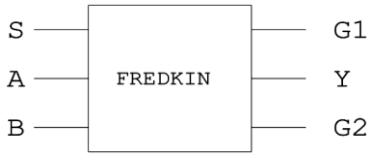


Figure 8. 2:1 reversible gate.

TABLE I. TRUTH TABLE OF REVERSIBLE FREDKIN GATE

S	*A*	*B*	*G1*	*Y*	*G2*
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

When the select input S=0, the output Y follows the input A, i.e Y=A, if the S=1, then the output Y follows the input B, i.e Y=B. G1 and G2 are the two garbage bits which is not required in multiplexing operation. However G1 follows the select input S, it may be used in additional circuits which requires the same input.

C. SAYEM GATE:

Sayem gate (SG) is a 4x4 reversible gate. The input and output vector of this gate are, Iv = (A, B,C,D) and Ov=(P,Q,R,S). The block diagram of this gate is shown in Fig 8. This gate can be used as a two input universal gate means it can perform any two input Boolean function. The sayem gate can be used to build reversible T- flip-flop along with Feynman gate.

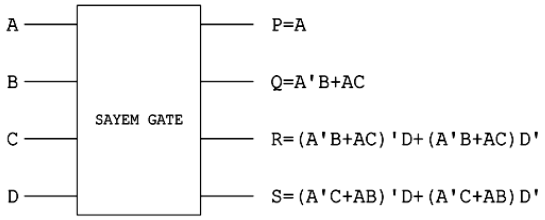


Figure 9. Sayem gate

1) TRANSISTOR IMPLEMENTATION

Fig. 10 shows the Transistor implementation of Sayem gate. Actually the Sayem Gate is the combination of Fredkin Gate (FRG) and Feynman Gate (FG), and so it can simultaneously generate three output functions (from Q, R and S). The output P is taken with a nmos transistor. It takes 29 transistors for proposed completely reversible implementation of the Sayem gate. The proposed implementation is suitable for forward as well as backward computation.

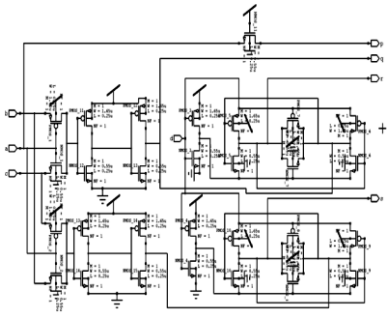


Figure 10. Reversible Transistor Implementation of the sayem gate.

2) LAYOUT:

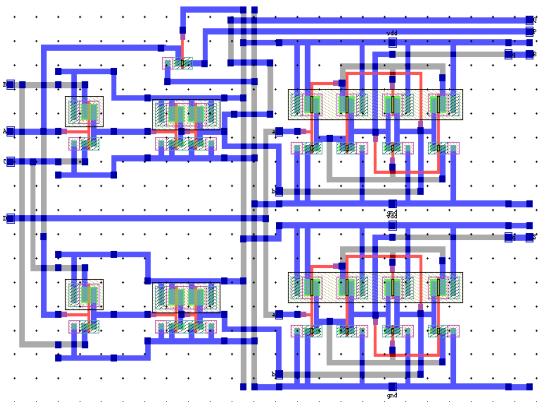


Figure 11. Layout of Reversible sayem gate.

D. URG GATE

URG gate is a 3x3 reversible gate. The input and output vector of this gate are,Iv=(A,B,C) and Ov=(P,Q,R).The block diagram of this gate is shown in Fig 11.This gate can be used in the binary to gray and gray to binary and also BCD to excess3 and excess3 to BCD converters.

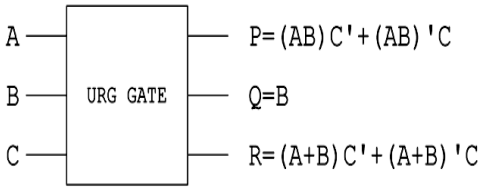


Figure 12. URG gate.

1) TRANSISTOR IMPLEMENTATION:

Fig. 13 shows the Transistor implementation of URG gate .It can simultaneously generate two output functions (from P and R). The output Q is taken with a nmos transistor. It takes 13 transistors for proposed completely reversible implementation of the URG gate. The proposed implementation is suitable for forward as well as backward computation.

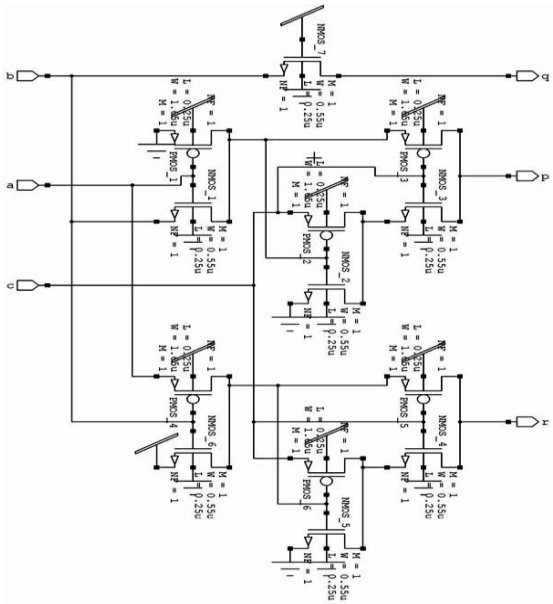


Figure 13. Reversible Transistor Implementation of the URG gate.

2) LAYOUT

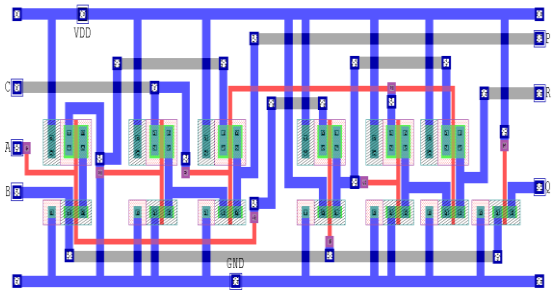


Figure 14. Layout of Reversible urg gate.

E. PROPOSED 8-BIT BARREL SHIFTER:

The diagram of barrel shifter shown in figure-13 the input is an 8-bit vector .The output is a shifted version of input, with the amount of shift defined by the "shift" input(0 to 7).the circuit consists of three individual barrel shifters. Notice that first barrel shifter has only one zero connected to one of the multiplexers (bottom left corner),while the second has two, and third has four. For larger vectors, we would just keep doubling the number of zero inputs. If shift=001,for example, then only the first barrel should cause a shift; on the other hand, if shift=111,then all barrels should cause a shift.

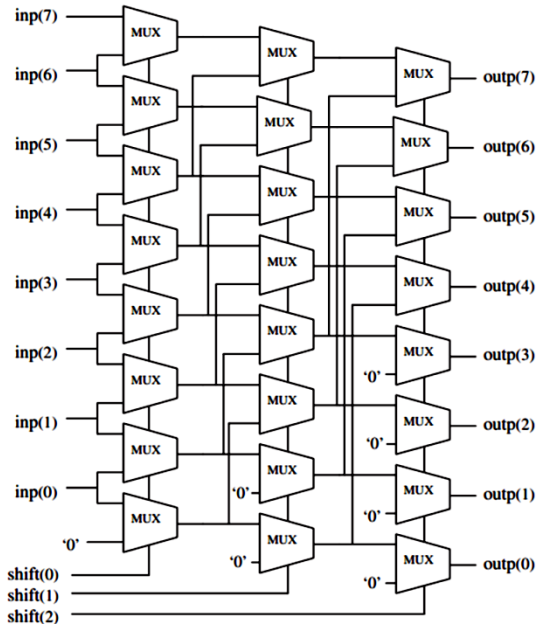


Figure 15. 8-bit barrel shifter.

The above figure considers first barrel shifter. In this case, the circuit must shift the input vector (of size 8) either 0 or 1 position to the left. when actually shifted (shift=1),the LSB bit must be filled with zero (shown in the bottom left corner of the diagram). If shift=0,output=input, if shift=1,then output(0)=0 and output(i)=input(i-1),1<i<7.

F. PROPOSED REVERSIBLE 8-BIT BARREL SHIFTER:

Reversible barrel shifter consists of fredkin gate as a main element. One of the application of the fredkin gate is it acts as a 2x1 multiplexer.a,b,c are the inputs and p,q,r as the out puts. We will take b,c as I0 and I1 and the input a acts as a selection line s. The output of this gate taken at q. And q output comes out as q=I0.S'+I1.S and p, r outputs can be acts as a garbage outputs. The reversible barrel shifter consists of three barrels connected in the fig. 16 as in the conventional one the reversible barrel shifter implemented with the replacement technique.

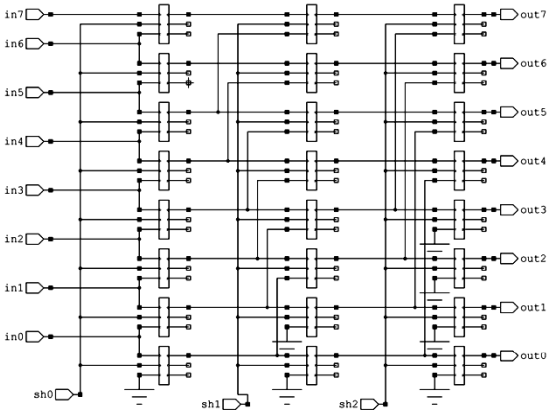


Figure 16. Reversible 8-bit barrel shifter.

G. LAYOUT

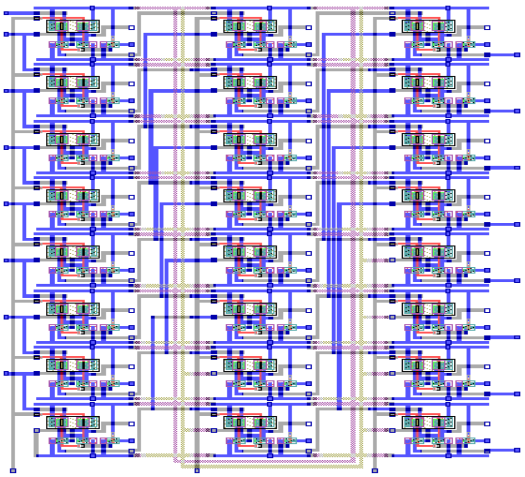


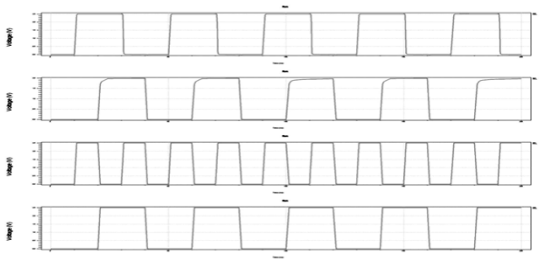
Figure 17. Layout of reversible 8-bit barrel shifter.

The layout of the 8-bit barrel shifter can be implemented with 4 metals and the widths of PMOS and NMOS are wp=1.65um,wn=0.55um with technology value 0.25um.It consists of 24 fredkin gates and 120 transisters with area of 1317.53μm².

IV. SIMULATION RESULTS

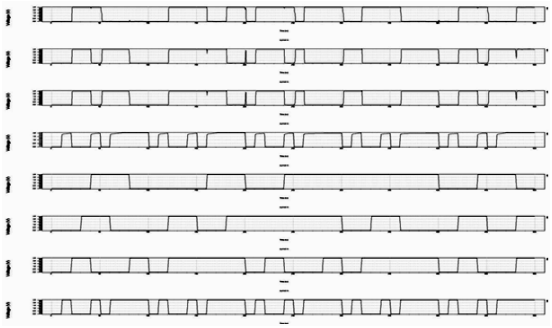
Simulation is based on TANNER TOOL V13. Graph presented below are input and output signal at respective input and output terminal at each gate.

A. Feynman gate:

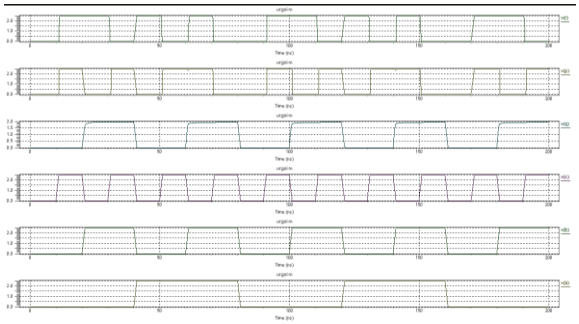


B. Fredkin gate

C. Sayem gate:

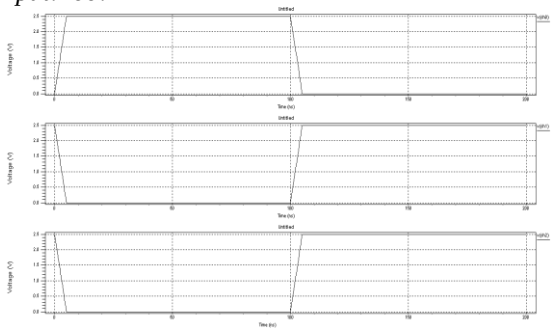


D. Urg gate:

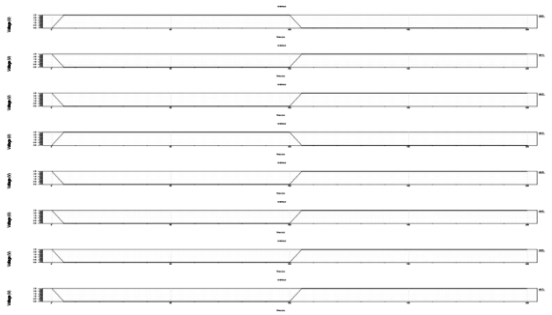


E. 8-bit barrel shifter :

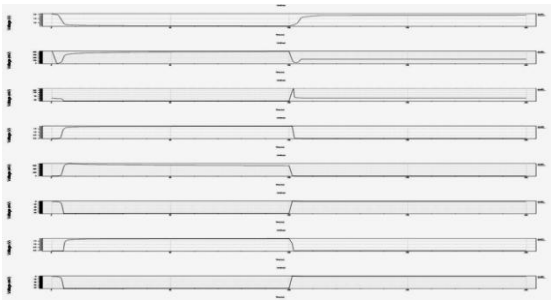
shift input:100.



Input:10010000.



Output:01001000



F. Comparisons of gates with power, delay, and area:

1.Power:

GATE	Avg Power dissipation(forward)	Avg Power dissipation(backward)
feynman	9.004727e-007 w	7.054828e-005 w
fredkin	3.859792e-007 w	3.662202e-007 w
sayem	5.187237e-007 w	5.551542e-004 w
urg	5.259238e-004 w	9.492534e-007 w

2.Delay :

GATE	delay(forward)	Delay(backward)
feynman	5.1651e-009 s	1.3522e-010 s
fredkin	2.6171e-009 s	5.5956e-009 s
sayem	3.0869e-008 s	4.7392e-008 s
urg	3.6059e-009 s	3.7685e-009 s

3.Area:

Module name	Area(μm²)
feynman	214.18
fredkin	110.863
sayem	241.753
urg	263.325
8-bit barrel shifter	1317.53

4. 8-bit barrel shifter:

	Avg power	delay
8-bit barrel shifter	2.265111e-007 w	1.7265e-009 s

V. CONCLUSION AND FUTUREWORK

Reversible logic is very important for low power and quantum circuit design. Most of the attempts on reversible logic design concentrate on reversible combinational logic design. Only a few attempts were made on reversible sequential circuit design. The major works on reversible sequential circuit design propose implementations of flip-flops and suggest that sequential circuit be constructed by replacing the flip-flops and gates of the traditional designs by their reversible counter parts. This method leads to reversible sequential circuits with higher realization costs and garbage outputs. As this is new approach to sequential circuit design using reversible gate. We made attempt to compare our design of different reversible circuits with respect to power dissipation factor. We observed that 8-bit barrel shifter has less power dissipation and delay, area of this counter is little bit more.

In future work, we plan to implement the reversible logic circuits with less area and less delay. Mostly these reversible

logic circuits can be implemented with pass transistor logics due to this threshold voltage drops we should not get the full swing levels at the output. so we need to redesign the gates to overcome these problems.

ACKNOWLEDGMENT

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